interleave adjustment, there is no fixed time period between the execution of steps 804 and 806. Rather, the controller is free to adjust the timing of step 806 relative to the timing of step 804 as needed to provide the desired interleave (e.g., to provide time to transmit the command control information for other transactions between execution of steps 804 and 806).

A3 end

IN THE CLAIMS:

Kindly **cancel** claims 1-~~41~~ 42 without prejudice.

Kindly **add** the following claims:

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1 (43) 42. A method of operation in a semiconductor memory device,
2 wherein the memory device receives an external clock signal and
3 includes an array of memory cells, the method comprises:
4 receiving a first code synchronously with respect to the
5 external clock signal, wherein the first code specifies that a
6 write operation is to be initiated in the memory device
7 receiving a second code synchronously with respect to the
8 external clock signal, wherein the second code specifies that a
9 precharge operation is to be initiated automatically after
10 initiation of the write operation;
11 detecting an external strobe signal, wherein the external
12 strobe signal indicates when to begin sampling data;
13 sampling the data upon detection of the external strobe
14 signal, wherein during the write operation, the memory device
15 writes the data to the array; and
16 initiating the precharge operation automatically after the
17 write operation is initiated.

1 (2 44) 43. The method of claim (1 43) 42 wherein a first portion of the
2 data is sampled synchronously with respect to the external clock
3 signal.

1 (3 45) 44. The method of claim (2 44) 43 further comprising sampling a
2 second portion of data synchronously with respect to the external
3 clock signal, wherein the first portion of data is sampled during
4 an odd phase of the external clock signal, and the second portion

of data is sampled during an even phase of the external clock signal.

45. The method of claim 44 wherein the first and second portions of data are both sampled during the same clock cycle of the external clock signal.

46. The method of claim 42 wherein the precharge operation is initiated after the memory device writes the data to the array.

47. The method of claim 42 wherein the external strobe signal is detected by sampling from an external signal line synchronously with respect to the external clock signal.

48. The method of claim 42 further comprising receiving address information synchronously with respect to the external clock signal.

49. The method of claim 48, wherein the address information and the data are received from a common set of external signal lines.

50. The method of claim 49 wherein the first code, second code and address information are included in a write request packet.

51. The method of claim 42 further comprising:

receiving a third code synchronously with respect to the

external clock signal, wherein the third code specifies that the memory device initiate a sense operation;

initiating the sense operation; and

activating a row of sense amplifiers during the sense operation.

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52. A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, the method comprises:

providing a plurality of control codes to the memory device wherein the plurality of control codes include a first code which specifies that a write operation be initiated in the memory device and a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation;

delaying for an amount of time after providing the plurality of control codes; and

issuing an external strobe signal to the memory device after delaying for the amount of time, to signal the memory device to sample data, wherein the data is to be written to the array during the write operation.

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53. The method of claim 52 further comprising issuing a first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

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54. The method of claim 53 wherein the first and second portions of the data are both issued during a first clock cycle of the external clock signal.

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55. The method of claim 52 further comprising:

issuing additional portions of the data to the memory device; and

issuing the external strobe signal to the memory device to signal the memory device to stop sampling data.

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56. The method of claim 52 further comprising providing address information to the memory device.

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57. The method of claim 56 wherein the plurality of control codes and the address information are both included in a first packet.

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58. The method of claim 57 wherein the data is included in a second packet and wherein the first packet and the second packet are transported over a common set of external signal lines.

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59. The method of claim 52 wherein the plurality of control codes includes a third code which specifies that a row of sense amplifiers be activated.

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60. A synchronous semiconductor memory device having an array which includes a plurality of memory cells, wherein the memory device receives an external clock signal, the memory device comprises:

a first input receiver to receive a first code synchronously with respect to the external clock signal, wherein, when the first code specifies a write operation, the memory device samples data upon detection of an external strobe signal;

a row of sense amplifiers coupled to the array, to store the data in the array during the write operation; and

a second input receiver to receive a second code synchronously with respect to the external clock signal, wherein the second code specifies that precharging the row of sense amplifiers occur automatically after the data is stored in the array.

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61. The memory device of claim 60 further comprising a clock generator circuit to receive the external clock signal, wherein the data is sampled synchronously with respect to the external clock signal.

21 63 19 61

62. The memory device of claim 60 further comprising a plurality of input receiver circuits to sample a first portion of the data and a second portion of the data, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

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63. The memory device of claim 62 wherein the first input receiver and the second input receiver are both included among the plurality of input receiver circuits.

64. The memory device of claim 62 wherein the plurality of input receiver circuits sample additional portions of data until detection of an external termination signal.

65. The memory device of claim 60 wherein the second input receiver samples address information synchronously with respect to the external clock signal.

66. The memory device of claim 60 further comprising a third input receiver to sample the external strobe signal.

67. The memory device of claim 60 wherein the first code and the second code are included in a packet.

68. The memory device of claim 60 further including a third input receiver to receive a third code synchronously with respect to the external clock signal, wherein the third code specifies that the row of sense amplifiers sense the contents of a row of memory cells included in the array.

69. The memory device of claim 68 wherein the data is stored in the row of memory cells included in the array during the write operation.

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70. A dynamic random access memory device which receives an external clock signal, the memory device comprises:

an array of memory cells;

a first input receiver to receive a first code synchronously with respect to the external clock signal, wherein the first code indicates that a write operation be initiated in the memory device;

a second input receiver to receive an external strobe signal, wherein receipt of the external strobe signal indicates when the memory device is to begin sampling data, wherein the data is to be stored in the array during the write operation; and

a third input receiver to receive a second code which specifies that a row of sense amplifiers be precharged automatically after the data is stored in the array, wherein the second code is received synchronously with respect to the external clock signal.

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71. The memory device of claim 70 further comprising a fourth input receiver to receive a third code synchronously with respect to the external clock signal, wherein the third code indicates that the row of sense amplifiers sense the contents of a row of memory cells of the array.

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72. The memory device of claim 71 wherein further comprising a plurality of input receivers to receive address information which identifies the row of memory cells, wherein the address information is received synchronously with respect to the external clock

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signal.

73. The memory device of claim 70 wherein the third input receiver also receives address information synchronously with respect to the external clock signal.

74. The memory device of claim 70 further comprising a plurality of input receiver circuits to sample a first portion of the data and a second portion of the data, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

75. The memory device of claim 74 wherein the first and second portions of the data are both sampled during a common clock cycle of the external clock signal.

76. The memory device of claim 70 wherein the first and second codes are included in a packet.

77. The memory device of claim 76 wherein the first and second codes are both included in a first packet and the data is included in a second packet.

78. The memory device of claim 77 wherein the first and second packet are multiplexed over a common set of external signal lines.